

EVR18282061

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. ..... 10/057,711  
Priority Filing Date ..... January 24, 2002  
Inventor ..... Warren M. Farnworth et al.  
Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2829  
Priority Examiner ..... R. Robert  
Attorney's Docket No. ..... MI22-2379  
TITLE: Method and Apparatus for Testing Semiconductor Circuitry for Operability and  
Method of Forming Apparatus for Testing Semiconductor Circuitry for Operability

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Commissioner for Patents  
Washington, D. C. 20231

**SUBSTITUTE DRAWING REQUEST**

Please enter the enclosed substitute formal drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: 7-31-03 By: D. Brent Kenady  
D. Brent Kenady  
Reg. No.: 40,045  
CUSTOMER No. 021567

Enclosures: 10 Sheets of Formal Drawings, Figs. 1-19.